

CLAIMS

What is claimed is:

1. A method of manufacturing a semiconductor device on a silicon-on-insulator wafer including a silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane, comprising the steps of:

forming at least one cavity through the silicon active layer in the at least one scribe lane;

forming at least one gettering plug in each said cavity, each said gettering plug comprising doped fill material containing a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

2. The method of claim 1, wherein the doped fill material is polysilicon formed by LPCVD deposition of the polysilicon and the dopant in the cavity.

3. The method of claim 1, wherein the dopant ions are one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

4. The method of claim 3, wherein the dopant is phosphorus.

5. The method of claim 1, wherein the step of forming at least one cavity further comprises forming a sidewall liner in the cavity.

6. The method of claim 1, wherein the gettering plug extends down through the silicon active layer, and contacts a dielectric insulation layer on the wafer.

7. The method of claim 1, wherein the gettering plug extends down through both a silicon active layer and a dielectric insulation layer on the wafer.

Docket No. F0556

8. The method of claim 7, wherein in the gettering step gettered impurities migrate into a silicon substrate layer below the dielectric insulation layer.

5 9. A method of gettering impurities on a silicon-on-insulator wafer including a silicon active layer having at least two die pads formed thereon, the at least two die pads separated by at least one scribe lane, comprising the steps of:

forming at least one cavity through the silicon active layer in the at least one scribe lane;

filling the cavity with a fill material;

10 adding at least one dopant to the fill material to form at least one gettering plug including a plurality of gettering sites; and

subjecting the wafer to conditions to getter at least one impurity into the plurality of gettering sites.

15 10. The method of claim 9, wherein the dopant ions are one or more selected from phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

20 11. The method of claim 9, wherein the step of forming at least one cavity further comprises forming a sidewall liner in the cavity.

12. The method of claim 10, wherein the fill material is polysilicon, and the dopant is added by one of codeposition and implantation.

25 13. The method of claim 10, wherein the gettering plug extends through the silicon active layer, and contacts a dielectric insulation layer on the wafer.

14. The method of claim 10, wherein the gettering plug extends through both the silicon active layer and a dielectric insulation layer on the wafer.

15. The method of claim 14, wherein in the gettering step gettered impurities move into a silicon substrate layer below the dielectric insulation layer.

5 16. A silicon-on-insulator semiconductor wafer comprising:
a silicon active layer;
a plurality of die pads formed in the silicon active layer;
at least one scribe lane between and separating adjacent die pads; and
at least one gettering plug in the at least one scribe lane, wherein the at least one gettering plug extends through the silicon active layer and the gettering plug comprises a doped fill material having a plurality of gettering sites.

10 17. The SOI semiconductor wafer of claim 16, wherein the gettering plug further comprises a sidewall liner separating the gettering plug from the adjacent die pad.

15 18. The SOI semiconductor wafer of claim 17, wherein the sidewall liner is a material selected from silicon dioxide, silicon oxynitride and silicon nitride

20 19. The SOI semiconductor wafer of claim 16, wherein the doped fill material is doped with one or more of phosphorus, arsenic, antimony, bismuth, boron, aluminum, gallium, indium, helium, neon, argon, krypton, xenon and germanium.

25 20. The SOI semiconductor wafer of claim 16, wherein the doped fill material is doped polysilicon.